BRIEF PAPER A 0.1–1 GHz CMOS Variable Gain Amplifier Using Wideband Negative Capacitance

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SUMMARY This Paper presents the design of a wideband variable gain amplifier (VGA) using $0.18 \,\mu$ m standard CMOS technology. The proposed VGA realizes wideband flat gain using wideband flat negative capacitance. It achieves a 3 dB gain bandwidth of 1 GHz with a maximum gain of 23 dB. Also, it shows P1 dB of -33 to -6 dBm over the gain range of -28 to 23 dB. The overall current consumption is 5.5 mA under a 1.5 V supply.

key words: variable gain amplifier, wideband, cascode, negative capacitance

1. Introduction

As digital RF and ultra-wideband (UWB) system become hot issues of the wireless transceiver design, the designs of front-end blocks become more demanding and have many challenges [1], [2]. Among them, the role of RF VGA becomes particularly important because it relieves the burden of wide dynamic range at the following stages. A VGA has two important characteristics to be successfully implemented in a wireless transceiver and do its function.

First, a VGA needs to realize dB-linear gain control by Vcnt, because it enables a wide gain control range and a short and constant settling time for an AGC circuit [3]. Fortunately, many papers report successful result of dB-linear gain control by Vcnt [4]–[6]. Second, a VGA should have a wide bandwidth to be successfully incorporated in the digital RF system using many frequency bands or a wideband system like UWB. Although many approaches for wideband VGA are introduced in many papers, the bandwidth is still insufficient. The major problem lies on the method of wideband realization.

There is a widely used method to attenuate the effect of output capacitance, which is the effective inductance technique using parallel resonance. However, it has a limit to realize a wideband VGA because of the frequency selective characteristics of parallel resonance [4], [5]. To solve this problem, we propose to use the negative capacitance technique which is very effective because the negative capacitance cancels capacitance directly. Some papers already used this negative capacitance technique to reduce the input capacitance and enhance the bandwidth of VGA [7], [8].

In this paper, we propose to apply this negative capaci-

tance technique to reduce the output capacitance of the VGA using a special structure which is called the negative capacitance generator in this paper. The VGA also realizes dBlinear gain control by Vcnt incorporating cascode structure and proper operation modes of FETs. The design's efficacy was verified with simulation and measurement results.

2. Design

2.1 Structure Review

The first consideration in deciding the structure of a VGA is a dB-linear gain control by Vcnt. Among the widely used structures for dB-linear gain control, we choose the cascode structure which needs no additional circuit. It consumes less power than other structures because it reuses the current and doesn't need any additional circuit for dB-linear realization. It achieves dB-linear gain control characteristics by designing common source amplifiers (M3, M4) to operate in linear mode, and common gate amplifiers (M1, M2) to operate in saturation mode [4].

Also, the wideband realization is an important consideration on deciding VGA structure and this is a focus of this letter. Conventional VGAs increase the bandwidth by using effective inductance. They diminish the effect of the output capacitance by parallel resonance with the effective inductance. However, parallel resonance cannot be effective over a wide frequency range because of its frequency selective characteristics. Besides, the output capacitance of the VGA is increased by additional circuitry used to realize effective inductance.

Thus, we propose to use the negative capacitance generator instead of the effective inductance. The negative capacitance generator is connected in parallel to the output capacitance as shown in Fig. 1, and reduces the effect of output capacitance. Because the negative capacitance reduces the output capacitance directly, not by the resonance, this technique is more appropriate for wideband realization than the conventional technique using the effective inductance. The bandwidth of the VGA using negative capacitance is limited only by the bandwidth of the negative capacitance generator, which is explained in the next section.

2.2 Negative Capacitance Generator

It is widely known that the negative capacitance can be generated by adding cross-coupling capacitors to the main am-

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Fig. 1 Schematic of the proposed wideband VGA.



Fig.2 Schematic and simulation result of the negative capacitance generator. (a) Schematic of the negative capacitance generator. (b) Simulated frequency response of the negative capacitance generator.

plifier [7]. However if we use this method, negative capacitance is hard to control because it is hard to change the gain of the main amplifier. Also, the parasitic capacitance caused by the cross-coupling capacitors connected to input/output reduces the bandwidth of the main amplifier. Thus, it is better to use negative capacitance generator separated with the main amplifier. There is a strong candidate structure for negative capacitance generator which is known as a relaxation oscillator. Also, the effectiveness of this structure as a negative capacitance generator was already reported [8]. However, this structure generates a negative resistance as well as a negative capacitance. Thus, there is a risk of oscillation and we cannot avoid the noise figure (NF) and the linearity degradation. To generate negative capacitance without these problems, we propose a negative capacitance generator as shown in Fig. 2. This structure is a simple commonsource amplifier with cross-coupled capacitors and parallel R-C pairs (R1-C1, R2-C2 in Fig. 2(a)). This structure is separated from the main amplifier and easy to control the negative capacitance. Also, it generates no negative resistance. Additionally, it uses parallel R-C pairs to enhance its bandwidth. These R-C pairs operate mainly as resistors at low frequencies, and mainly as capacitors at high frequencies. Thus, they decrease gain only at low frequencies by source degeneration of R and realize wideband flat gain as in Fig. 2(b).



Fig. 3 Simulated negative capacitance with four cross-coupling capacitors. (a) 200 fF (with 5.5 dB gain, 0.72 mA). (b) 160 fF (with 7 dB gain, 1.0 mA). (c) 120 fF (with 10 dB gain, 1.88 mA). (d) 80 fF (with 12 dB gain, 2.35 mA).

In design of the negative capacitance generator, the selection of C_{CC} (cross-coupling capacitance) and A_{DA} (differential amplifier gain) is important because they affect the gain flatness and power consumption of the differential amplifier. The smaller choice is the better for both of these values. First, a smaller value of C_{CC} helps to maintain the wideband flat gain of the differential amplifier by reducing output capacitance of the amplifier. Also, a smaller value of A_{DA} helps to reduce the power

$$C_{eff} = \frac{Q_{eff}}{V_s} = \frac{(1 - A_{DA}) \cdot V_s \cdot C_{CC}}{V_s} = (1 - A_{DA}) \cdot C_{CC} \quad (1)$$

consumption. However, the value of C_{CC} and A_{DA} should be decided to make the required Q_{eff} (effective charge) and C_{eff} (effective capacitance) as in Eq. (1). Thus, we cannot avoid the tradeoff between C_{CC} and A_{DA} .

Figure 3 shows four negative capacitance graphs over 0.1-2 GHz which are made by four different combinations of C_{CC} and A_{DA}. Though 160 fF with 7 dB gain is enough to realize flat negative capacitance over 0.1-1 GHz, we choose 120 fF with 10 dB gain to keep some margin considering parasitic capacitance although it consumes extra power. As shown in Fig. 4, negative capacitance generator using 120 fF with 10 dB gain reduces the output capacitance of the VGA to 20 fF over the 0.1-1 GHz frequency range as Fig. 4(b), and realizes wideband VGA for 0.1-1 GHz.

3. Measurement Results

The proposed VGA was fabricated using $0.18 \,\mu\text{m}$ CMOS technology. The active area for the VGA is $275 \,\mu\text{m} \times 187 \,\mu\text{m}$ as shown in the die photograph of Fig. 5. The VGA consumes 5.5 mA under 1.5 V VDD without a buffer. The performance of the VGA is measured with a signal source generator (Agilent E4438C) and a spectrum analyzer (Agilent E4440A). The V_{cnt} - Gain curve in Fig. 6 shows dB-linear gain control characteristics of the VGA with a gain control range of -28 to 23 dB. And the V_{cnt} - P1 dB curve in Fig. 6 shows a P1 dB range of -33 to -6 dBm. The P1 dB variation over the 0.1–1 GHz frequency range is below 1 dB for every gain settings. Also, the V_{cnt} - NF curve in Fig. 7 shows a NF



Fig.4 Simulated total output capacitance of VGA. (a) Without negative capacitance generator. (b) With negative capacitance generator $(C_{CC}=120 \text{ fF}, A_{DA}=10 \text{ dB}).$



Fig. 5 Die photograph of the proposed wideband VGA.



Fig. 6 Measured Vcnt-P1 dB/Gain curve of VGA at 500 MHz.

range of 3.9 to 39 dB. The NF@ maximum gain ranges from 3.9 to 5.2 dB over the 0.1–1 GHz frequency range. Finally, the 3 dB bandwidth of the VGA for maximum gain is 1 GHz as shown in Fig. 8.

4. Conclusion

A newly proposed VGA was fabricated using $0.18 \mu m$ CMOS technology. We propose the new VGA design technique using negative capacitance generator. The negative capacitance generator directly cancels the output capacitance of VGA and realizes wideband flat gain. It would overcome the problem of parallel resonance which shows frequency selective characteristics. Also, the VGA incorporates a cascode structure to realize a dB-linear gain control characteristics and current reuse.



Fig. 7 Measured Vcnt-NF curve of VGA at 500 MHz.



Fig. 8 Measured Freq-Gain curve of VGA for various Vcnt.

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References

- R. Bagheri, A. Mirzaei, M.E. Heidari, S. Chehrazi, M. Lee M. Mikhemar, W.K. Tang, and A.A. Abidi, "Software-defined radio receiver: Dream to reality," IEEE Commun. Mag., vol.44, no.8, pp.111– 118, Aug. 2006.
- [2] I.D. O'Donnell and R.W. Brodersen, "An ultra-wideband transceiver architecture for low power, low rate, wireless systems," IEEE Trans. Veh. Technol., vol.54, no.5, pp.1623–1631, Sept. 2005.
- [3] J.M. Khoury, "On the design of constant settling time AGC circuit," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol.45, no.3, pp.283–294, March 1998.
- [4] H.D. Lee, K.A. Lee, and S. Hong, "Wideband VGAs using a CMOS transconductor in triode region," Proc. 36th European Microwave Conference, pp.1449–1452, Sept. 2006.
- [5] H.D. Lee, K.A. Lee, and S. Hong, "A wideband CMOS variable gain amplifier with an exponential gain control," IEEE Trans. Microw. Theory Tech., vol.55, no.6, pp.1363–1373, June 2007.
- [6] Q.-H. Doung, T.K. Nguyen, and S.-G. Lee, "CMOS exponential current-to-voltage circuit based on newly proposed approximation method," Proc. International Symp. on Circuits and Systems II, pp.23– 26, May 2004.
- [7] F. Aznar, S. Celma, B. Calvo, and D. Digon, "A fully integrated inductorless AGC amplifier for optical gigabit ethernet in 0.18 μm CMOS," IEEE International Symp. on Industrial Electronics, pp.1662–1667,

July 2008 [8] S. Galal and B. Razavi, "40-Gb/s amplifier and ESD protection circuit in 0.18- μ m, CMOS technology," IEEE J. Solid-State Circuits, vol.39, no.12, pp.2389–2396, Dec. 2004.